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## Introduction

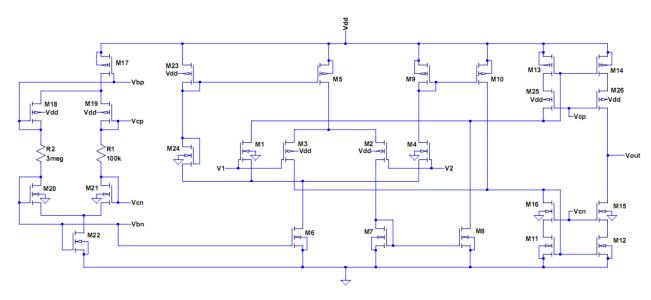
For the final project in ENGR 2420: Introduction to Microelectronic Circuits, we were asked to design a rail-to-rail CMOS differential amplifier with the following specifications:

- rail-to-rail output voltage swing
- rail-to-rail common-mode input voltage range
- DC gain in excess of 60 dB for all common-mode input voltages within 0.5V of each rail
- unity-gain crossover frequency of at least 100 kHz while driving a 100-pF load capacitor
- unity-gain stable while driving a 100-pF load capacitor
- the small-amplitude step response should exhibit no overshoot and ringing while driving a 100pF load capacitor

In addition, it should behave similarly over the complete range of common-mode input voltages and consume as little power as possible. My design builds off of the current-mirror differential amplifier we have created in Lab 9, adding a couple "cascode current mirrors," creating a constant- $g_m$  rail-to-rail input stage, and adding the appropriate bias circuitry. This report briefly outlines the design and simulated results.

Note that all simulations were done in LTSpice using the supplied MOS transistor models (00linNMOS and 00linPMOS). nMOS transistors were 10  $\mu$ m wide and 1  $\mu$ m long while pMOS transistors were 14  $\mu$ m wide and 1  $\mu$ m long.

## **Schematic**



#### **Power**

To get a measure of how efficient our amplifier is, we simulated the current drawn by the amplifier when it was connected as a unity gain follower with the input in the middle of the rails. For  $V_{dd}$ =5 V, we measured a quiescent current of 113.3  $\mu$ A ( $V_1$ =2.5 V). Note that for  $V_{dd}$ =3.3 V, the circuit draws only draws 48.8  $\mu$ A.

### **Demonstrations**

Figure 1 shows the results when sweeping  $V_1$  from 0 to +5 V, for many values of  $V_2$  that span the entire rail-to-rail input range. Note the rail-to-rail output swing over the entire range. The response is also identical over the entire input range.

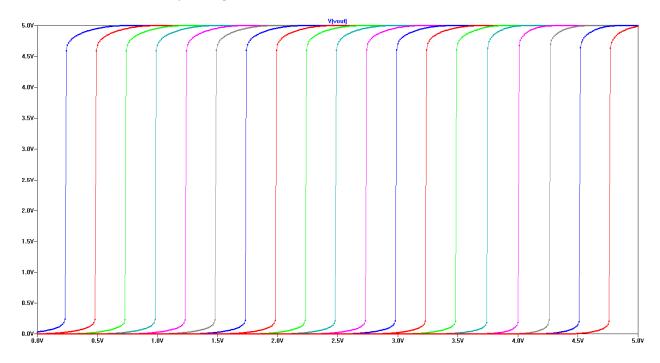


Figure 1: DC Sweep of Inputs

Figure 2 shows a sweep of  $V_1$  around 0.5 V. From this we can find the DC gain by looking at the slope (derivative) of the line in the high-gain region. The red line in the plot is the derivative, showing a gain of several thousand in the high-gain region. Similarly, Figure 3 shows the DC gain around 4.5 V. Similar tests were done to show that the gain is above 60 dB (1000x) for all common mode input voltages within 0.5V of the rails.

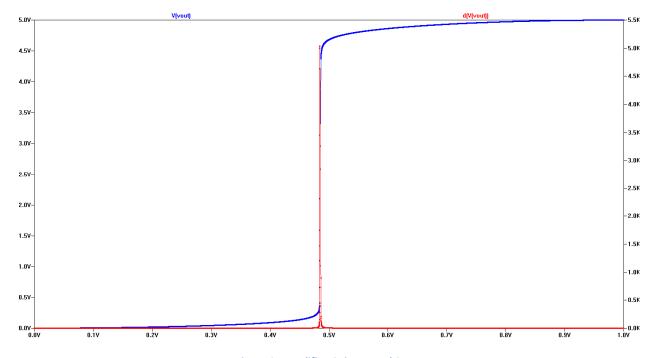


Figure 2: Amplifier Gain around 0.5 V

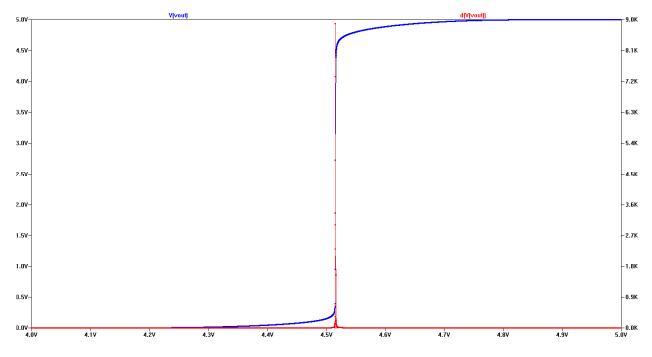


Figure 3: Amplifier Gain around 4.5 V

We then set up our simulated circuit as a unity gain follower driving a 100 pF capacitor. The voltage transfer characteristic of this follower is shown in Figure 4. Note the linear response over the entire range.

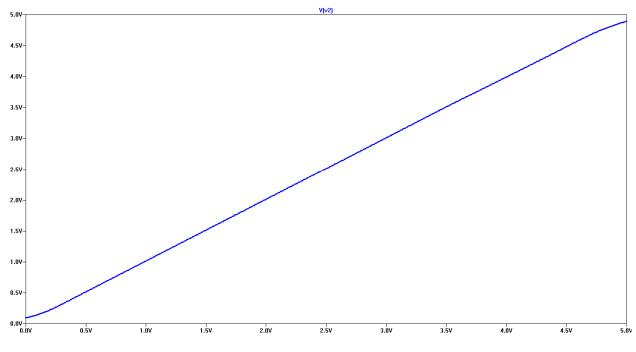
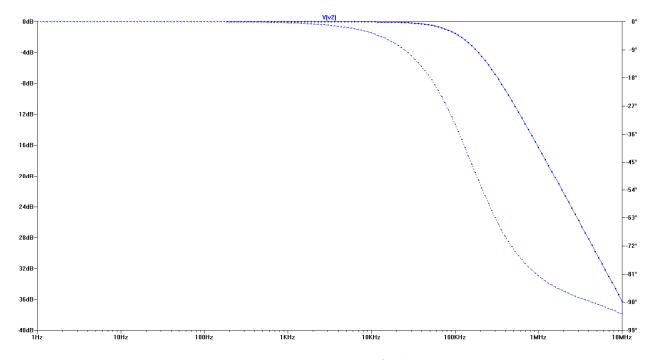


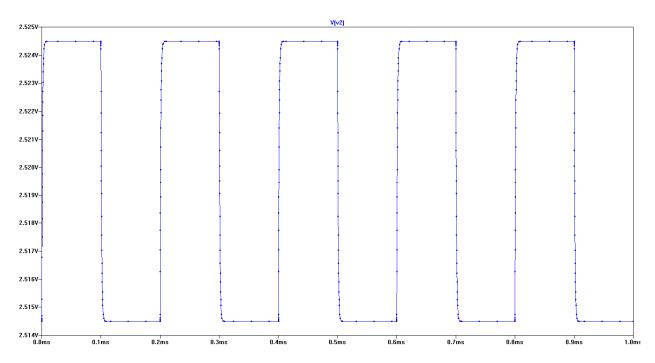
Figure 4: Unity Gain Response

Figure 4 shows the frequency response of the unity gain follower while driving a 100 pF capacitor. The circuit has a gain of 1 (0 dB) as expected over most of the range. The crossover frequency is clearly greater than 100 kHz as specified.



**Figure 5: Frequency Response of Follower** 

Figures 5 and 6 show the follower's response to a small signal square wave. Note that the response is stable and does not overshoot or ring.



**Figure 6: Square Wave Response of Follower** 

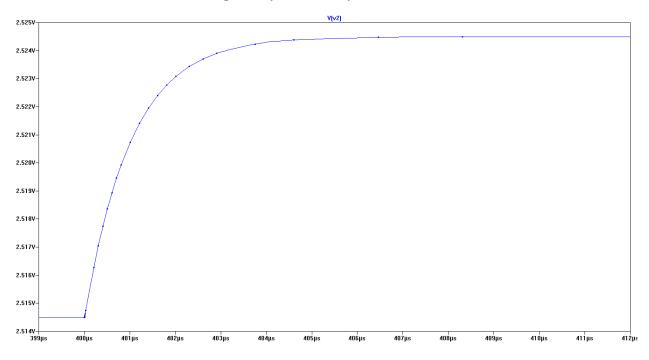


Figure 7: Smooth Step Response

These tests demonstrate that the differential amplifier meets all of the specifications outlined in the lab.

# **Appendix**

The LTSpice files are attached. If there are any questions about this report or the contained material, please email me at <a href="mailto:raphael.cherney@students.olin.edu">raphael.cherney@students.olin.edu</a>.